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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/560,677
Filing Date: December 14, 2005
Appellant(s): CUPPENS, ROGER

Thomas h. Ham
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 01/05/2009 appealing from the Office action mailed 08/04/2008.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4,527,255 A1 Keshtbod, 07-1985

6,363,011 B1 Hirose et al. 03-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. **Claims 1-5, 7-12** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Keshtbod** (US Patent 4,527,255) in view of **Hirose et al.** (US Patent 6,363,011 B1).

6. ***Regarding Independent claim 1***, Keshtbod teaches a static memory (**Fig. 2, Q1, Q2**) defining at least first and second nodes (**Fig. 2, N1, N2**) communicatively connected with read and/or write data lines (**Fig. 2, #23, #24**);

at least one non-volatile memory (**Fig. 2, Q3, Q4**) associated with the static memory

(**Fig. 2, Q1, Q2**), and writing data stored therein to the static memory (**Fig. 2, Q1, Q2**); the non-volatile memory (**Fig. 2, Q3, Q4**) comprising a first non-volatile element (**Fig. 2, Q3**) having a control gate connected to a first node (**Fig. 2, N2**) and a source connected to a second node (**Fig. 2, N1**), and a second non-volatile element (**Fig. 2, Q4**) having a control gate connected to the second node (**Fig. 2, N1**) and a source connected to the first node (**Fig. 2 N2**), the drain of each non-volatile element (**Fig. 2, Q3, Q4**) being connected by of a respective transistor (**Fig. 2, Q5, Q6**) to a supply voltage; characterized in that the respective transistors (**Fig. 2, Q5, Q6**) are arranged to isolate the drains (**Fig. 2 D3, D4**) of the first and second non-volatile elements from the supply during a program cycle of the memory device (**Fig. 2, #30**).

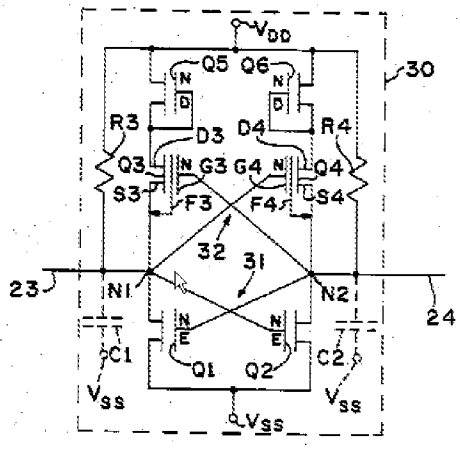

Fig. 2

Keshtbod is silent with respect to the static memory means comprises a pair of cross-coupled inverters.

Hirose et al. teaches the static memory (**Fig. 4, #4**) means comprises a pair of cross-coupled inverters (**Fig. 1, #45, #45'**).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of **Hirose et al.** to the teaching of **Keshtbod** such that the reading process of six transistors SRAM cells is easier than four transistors SRAM cells.

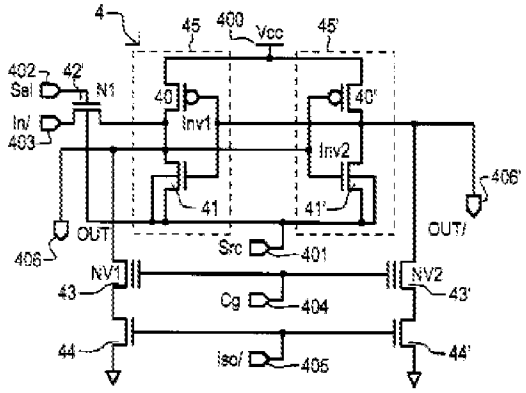

Fig. 5

7. ***Regarding claim 2***, Keshtbod teaches the non-volatile memory elements (**Fig. 2, Q3, Q4**) comprise embedded flash or EEPROM elements (**Abstract, lines 3-5**).

8. ***Regarding claim 3***, Keshtbod teaches the non-volatile memory elements (**Fig. 2, Q3, Q4**) comprise double or single poly floating gate type memory cells (**Abstract, lines 3-5**).

9. ***Regarding claim 4***, Keshtbod teaches the non-volatile memory elements (**Fig. 2, Q3, Q4**) comprise devices, which can be programmed and erased by of tunneling of

charges (**column 4, lines 58-61**).

10. ***Regarding claim 5***, Keshtbod teaches the non-volatile memory elements (**Fig. 2, Q3, Q4**) are programmed with opposite data (**column 7 lines 1-3, 13-15**).

11. ***Regarding claim 7***, Keshtbod teaches one or more respective selection transistors (**Fig. 1, Q7, Q8**) are provided, by of which the nodes (**Fig. 1, Fig. 2, #23, #24**) are communicatively coupled to the read and/or write lines (**Fig. 1**).

12. ***Regarding claim 8***, Keshtbod teaches respective selection transistors (**Fig. 1, Q7, Q8**) are including one or more isolation transistors (**Fig. 1, Q7, Q8**).

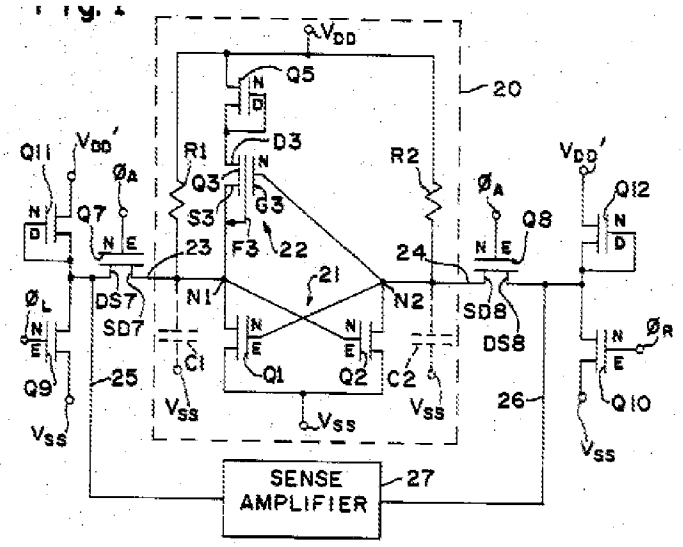

Fig. 1

13. ***Regarding claim 9***, Keshtbod teaches reconfigurable programmable logic device (**Fig. 4, column 10, lines 8-16**).

14. ***Regarding claim 9***, Keshtbod teaches a field programmable gate array including a memory device (**Fig. 4, column 10, lines 8-16**).

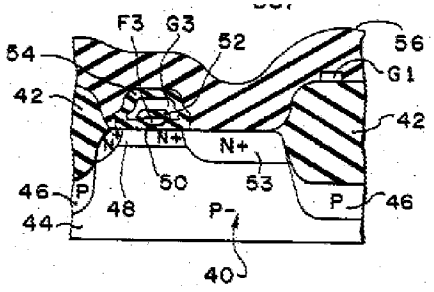

Fig. 4

15. ***Regarding claim 11,*** Keshtbod teaches all of the limitation s discussed above (from which these claims depend).

Keshtob is silent with respect to gates of the respective transistors are connected together to receive a common signal.

Hirose et al. teaches gates of the respective transistors are connected together to receive a common signal (**Fig. 5, #404**).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of **Hirose et al.** to the teaching of **Keshtob** such that it's easy to control nonvolatile memory cells with common wordline.

16. ***Regarding claim 12***, Keshtbod teaches all of the limitation s discussed above (from which these claims depend).

Keshtbod is silent with respect to each of the cross-coupled inverters includes a pair of transistors, gates of the transistors of a first inverter of the cross-coupled inverters being connected to the second non-volatile element, gates of the transistors of a second inverter of the cross-coupled inverters being connected to the first non-volatile element.

Hirose et al. teaches each of the cross-coupled inverters (**Fig. 4, #45, #45'**) includes a pair of transistors (**Fig. 7, Inv1, Inv2**), gates of the transistors of a first inverter of the cross-coupled inverters being connected to the second non-volatile element (**Fig. 4, gate of 40 and 41 connect to #43'**), gates of the transistors of a second inverter of the cross-coupled inverters being connected to the first non-volatile element (**Fig. 9, gate of 40' and 41' connect to #43**).

It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the teachings of Hirose et al. to the teaching of Keshtbod such that the reading process of six transistors SRAM cells is easier than four transistors SRAM cells.

(10) Response to Argument

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For claim 1, the appellant argues that the examiner has failed to establish a *prima facie* case of obviousness for the independent claim 1, and the independent claim 1 cannot be rendered obvious in view of the cited reference of Keshtbod and Hirose et al.

Based on appellant's interpretation the examiner's prior arts cannot over come ***the static memory means comprise a pair of cross-coupled inverters***. The examiner disagrees.

According to appellant's art, a *cross-coupled inverter static memory* (**appellant's art, Fig. 1**) paired with two floating gate memories (**appellant's art, Fig. 3, #14, #16 as an example**)

Based on the examiner's interpretation, Keshtbod uses *cross-coupled transistors SRAM* (**Fig. 2, Q1, Q2**) paired with two floating gate memories (**Fig. 2, Q3, and Q4**). Keshtobod is silent with respect to a *cross-couple inverters type SRAM*.

Hirose et al. teaches a *cross-coupled inverter SRAM* (**Fig. 5, #45, #45'**) paired with two floating gate memories (**Fig. 5, #43, #43'**)

Any one who has ordinary skill in the art would recognized that the SRAM is a common technology in the memory field, the SRAM either has cross-coupled inverter or cross-coupled transistors, and they are all bi-stable memory cells (any memory circuit has ability to assume two stable states---0 or 1, for example.) The cross couple inverter comprises two inverter output connects to each others input like Fig. A shown below

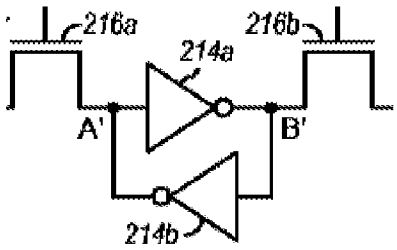

Fig. A

In the circuit layout diagram, the cross-coupled inverter in Fig. A can be draw as Fig.B wherein #45 are one inverter which equivalent to #214a in Fig. A, and #45' are another inverter which equivalent to #214b in Fig. A

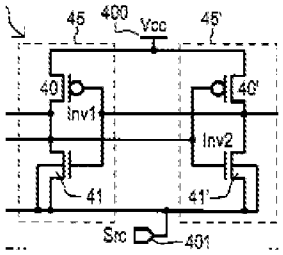

Fig. B

The cross-coupled inverter (six transistors) SRAM offers better and easy electrical accessing performance than cross-coupled transistors (four transistors) such as less noise, faster speed, less power, quicker transistors pull down time. On the other hand, the cross-coupled transistors SRAM offers smaller size in semiconductor design. However, both designs could be used as a static random access memory cell, and it's just different design choice.

The cross-coupled inverters are very commonly used and well known technology in the SRAM field, and it is not something new in the art. Any one who has ordinary skill in the art would recognize the cross-coupled inverter and cross-coupled transistors are inter-changeable.

For claims, 2-5, 7-12, the applicant argues the principal of operation of the bi-stable memory cell would change.

The examiner disagrees, as the examiner described previously, a bi-stable memory cell is a memory cell could assume two stable states---0 or 1. Like Keshtbod, Hirose also have SRAM and flash memories would assume two stable states--0 or 1, one who has ordinary skill in the art knew that weather having a single or separate control lines for control transistors would not change the basic principle of how the SRAM and flash memory cell stores data. Transistors Q5 and Q6 in the Keshtbod are acting like two load transistor which has less control ability. Hirose et al. have two transistor shared with a single control signal, which would be able to turned on/off two transistors at same time, and make two control transistors more flexablity. However the storage principal for SRAM and flash memory is not effect by these control transistors, since the main structure of the memory cell are same.

For the above reasons, it is believed that the rejections should be sustained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Respectfully submitted,

Han Yang

Conferees:

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